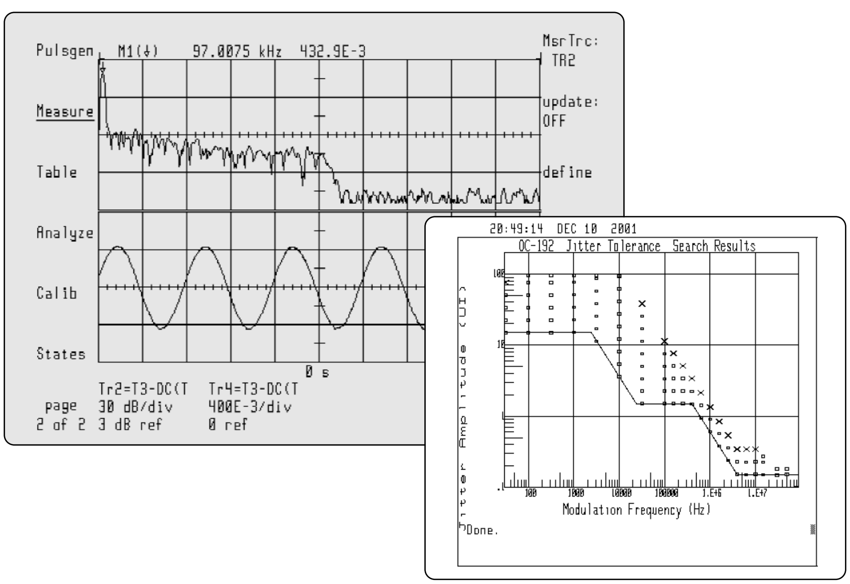
Frequency Agile Jitter Measurement System

Application Note 1267



Agilent Technologies

Contents

Introduction

This application note focuses on jitter measurements of components and equipment that make up synchronous networks such as the synchronous digital hierarchy (SDH) and the synchronous optical network (SONET). First, jitter is described, along with a discussion on why it is important. Next, jitter conformance tests are described, followed by a comparison of jitter measurement techniques. Finally, the measurement contributions of a frequency agile jitter measurement solution with diagnostic capability will be presented.

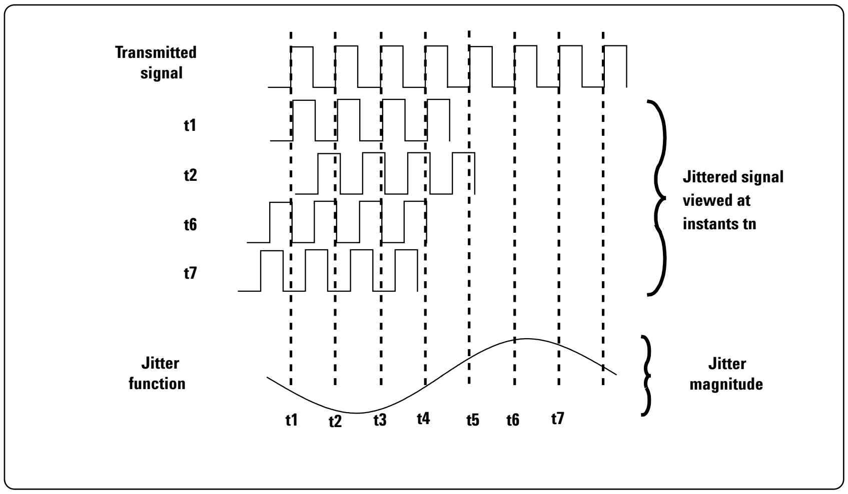


Figure 1. Jitter function

What is jitter?

ITU-T G.701 defines jitter as short-term non-cumulative variations of the significant instants of a digital signal from their ideal positions in time. The significant instant can be any convenient, easily identifiable point on the signal such as the rising or falling edge of a pulse or the sampling instant.

A second parameter closely related to jitter is wander. Wander generally refers to long term variations in the significant instants. There is no clear definition of the boundary between jitter and wander, however phase variations below 10 Hz are normally called wander.

Deriving the jitter function

Figure 1 shows an ideal pulse train compared at successive instants t_n with a real pulse train which has some timing jitter. By plotting the relative displacement in the instants, the jitter function is obtained. Typically, the jitter function is not sinusoidal. In addition to the jitter time function, the jitter spectrum could be displayed in the frequency domain.

The Unit Interval (UI)

Jitter amplitude is traditionally measured in unit intervals (UI), where 1 UI is the phase deviation of one clock period. The peak to peak UI deviation of the phase function with respect to time is referred to as the jitter amplitude. Since this is normalized to the clock period, it is independent of bit rate. It is therefore possible to compare jitter amplitude at different hierarchical levels in a digital transmission system. (Figure 2)

Controlling jitter is important because jitter can degrade the performance of a transmission system introducing bit errors and uncontrolled slips in the digital signals. Jitter causes bit errors by preventing the correct sampling of the digital signal by the clock recovery circuit in a regenerator or line terminal unit. In addition, jitter can accumulate in a transmission network depending on the jitter generation and transfer characteristics of the interconnected equipment.

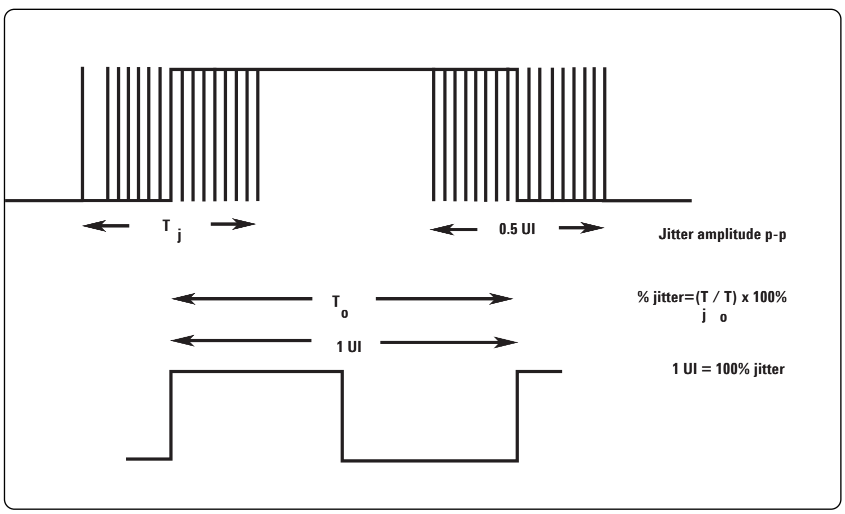


Figure 2. Definition of UI

Categories of jitter measurement

- Jitter tolerance
- Jitter transfer
- Jitter generation

There are several categories of jitter measurement. Jitter tolerance is defined in terms of an applied sinusoidal jitter component whose amplitude, when applied to an equipment input, causes a designated degradation in error performance. Jitter transfer is the ratio of the amplitude of an equipment's output jitter relative to an applied sinusoidal jitter component. Jitter generation is a measure of the jitter at an equipment's output in the absence of an applied input jitter. A related jitter noise measurement is output jitter, which is a measure of the jitter at a network node or output port.

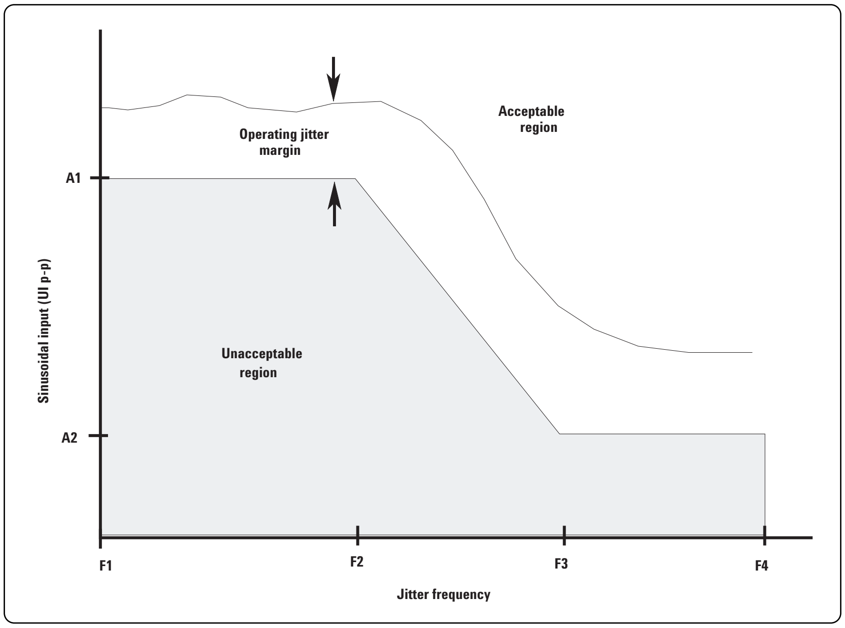
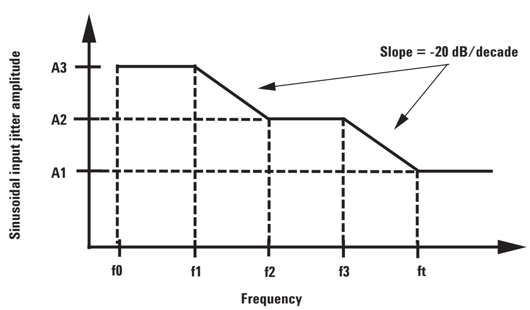


Figure 3. Jitter tolerance template



1 OC/STS-N	2 STM-N	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)	A1 (UI p-p)	A2 (UI p-p)	A3 (UI p-p)
1		10	30	300	2	20	0.15	1.5	15
3		10	30	300	6.5	65	0.15	1.5	15
	1(A)				6.5	65	0.15	1.5	
12		10	30	300	25	250	0.15	1.5	15
	4(A)				25	250	0.15	1.5	
24		10	200	2000	2	20	0.15	1.5	15
48		10	600	6000	100	1000	0.15	1.5	15
	16(A)				100	1000	0.15	1.5	
	16(B)				1.2	12	0.15	1.5	
192		10	2000	20000	400	4000	0.15	1.5	15

1. GR-253-CORE
2. ITU-T G958

Figure 4. Input jitter tolerance specification

Jitter tolerance measurement and template

Equipment jitter tolerance performance is specified with jitter tolerance templates. Each template defines the region over which the equipment must operate without suffering the designated degradation in error performance. The difference between the template and actual equipment tolerance curve represents the operating jitter margin, and determines the pass/fail status. (Figure 3)

Each transmission rate typically has its own input jitter tolerance template. In some cases, there may be two templates for a given transmission rate to accommodate different regenerator types. In addition, different standards may have different templates at similar rates. Shown here are the input jitter tolerance specifications for SONET and SDH transmission systems. (Figure 4)

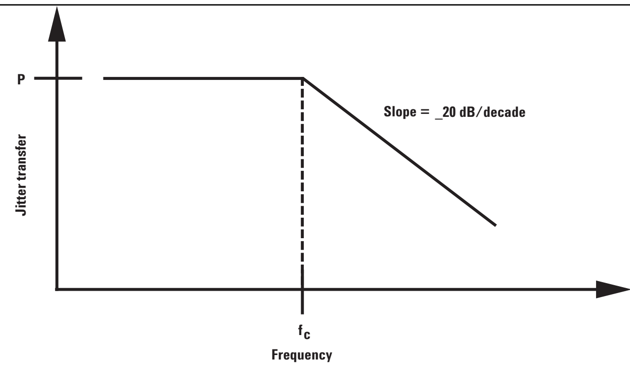
Jitter transfer specification

The jitter transfer function is also specified for each transmission rate and regenerator type. Jitter transfer requirements on clock recovery circuits specify a minimum amount of jitter gain versus frequency up to a given cut-off frequency, beyond which the jitter must be attenuated. The jitter transfer specification is intended to prevent the buildup of jitter in a network consisting of a cascade of regenerators. (Figure 5)

Jitter generation specification

Jitter generation is essentially a phase noise measurement and for SONET/SDH equipment is specified not to exceed 10 mUI rms when measured using a highpass filter with a 12 kHz cut-off frequency.

Although similar to jitter generation, the output jitter of the network ports is specified somewhat differently, as shown in Figure 6. Notice that for a given transmission rate the output jitter is specified in terms of peak- to- peak UI over two different bandwidths.



1 OC/STS-N	2 STM	f_c (kHz)	P (dB)
1		40	0.1
3	1(A)	130	0.1
12	4(A)	500	0.1
24		40	0.1
48 (A)	16(A)	2000	0.1
48 (B)	16(B)	30	0.1
192		120	0.1

1. GR-253-CORE
2. ITU-T G958

Figure 5. Jitter transfer specification

		Output jitter limit (UI p-p)		Measurement filter bandwidth corresponds to a band pass filter having lower cut-off frequency F_1 or F_3 and minimum upper cut-off frequency F_4		
STS level	OC level	Band 1 F_1 to F_4	Band 2 F_3 to F_4	F_1 (Hz)	F_3 (kHz)	F_4 (MHz)
1	1	1.5	0.15	100	20	0.4
3	3	1.5	0.15	500	65	1.3
(N/A)	12	1.5	0.15	1000	250	5
	24	1.5	0.15	2000	20	10
	48 (with type A regenerators)	1.5	0.15	5000	1000	20
	48 (with type B regenerators)	1.5	0.15	5000	12	20
	192	1.5	0.15	20000	4000	80

Figure 6. STS-n and OC-n output jitter specification

1. Oscilloscopes.
2. Phase detectors.
3. Sampling techniques with digital signal processing.
4. Dedicated SONET/SDH jitter analysis (including payload mapping and pointer adjustments).

Shown here are the most frequently encountered techniques to measure jitter. The first three techniques apply primarily to the measurement of jitter transfer and generation. Though the tests are applied to digital data, they tend to be analog in nature.

There are additional jitter measurements that deal with asynchronous data being mapped into the SONET/SDH format. Tests that examine the jitter due to payload mapping and pointer adjustments are performed by dedicated SONET/SDH testers, and are beyond the scope of this application note.

Jitter measurements using an oscilloscope

Intrinsic data jitter, intrinsic clock jitter, or jitter transfer can be directly measured with a high-speed digital sampling oscilloscope such as the 86100B Infiniium DCA. As shown in Figure 7, a jitter free-trigger signal for the oscilloscope is provided by clock source B, whose frequency reference is locked to that of clock source A. Clock source A, which is modulated by the jitter source, drives the pattern generator, which supplies jittered data for the jitter transfer measurement to device under test (DUT). The jittered input and output waveforms can be analyzed using the built-in oscilloscope histogram functions.

The limitations of the oscilloscope measurement technique are listed here. The maximum jitter amplitude that can be measured is limited to 1 UI peak-to- peak. Above this level, the eye diagram is totally closed. This technique offers poor measurement sensitivity, because of the inherently high noise level, due to the large measurement bandwidth involved. In addition, the technique does not provide any information about the jitter spectral characteristics or time domain waveform. Finally, the technique requires an extra clock source to provide the oscilloscope trigger signal.

Jitter measurement using phase detector

Many of the limitations of the sampling oscilloscope technique can be addressed using a phase detector. The phase detector compares the phase of the recovered clock from the device or equipment under test with a jitter free clock source. The output of the phase detector is a voltage that is proportional to the jitter on the recovered clock signal. The range of the phase detector can be extended beyond 1 UI by using a frequency divider. Intrinsic jitter is measured with appropriate bandpass filters.

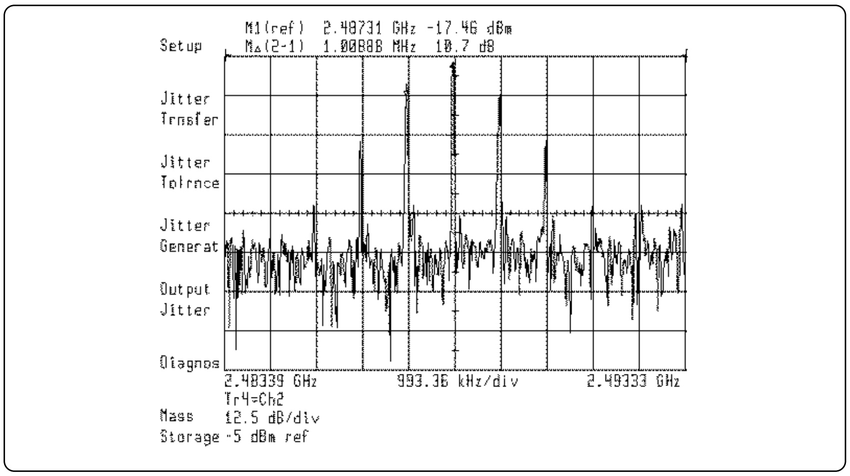


Figure 7. Configuration when using a sampling oscilloscope

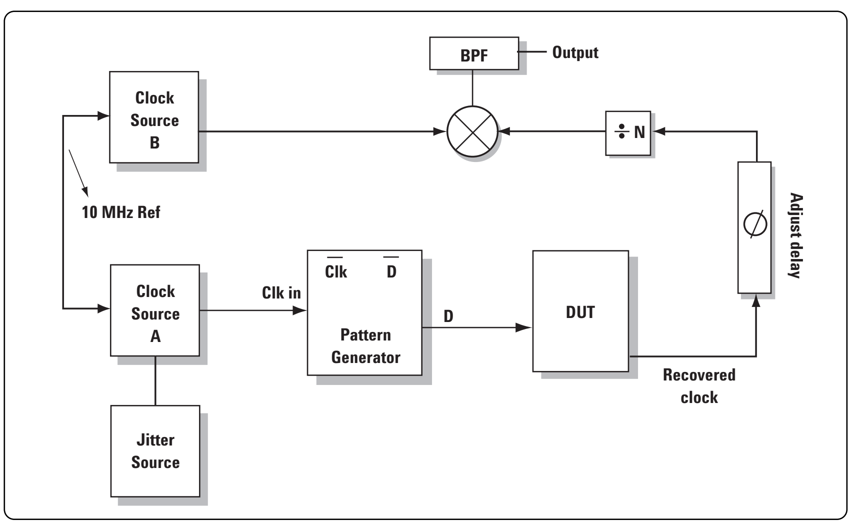


Figure 8. Configuration when using a phase detector

The phase detector method forms the basis for most dedicated jitter measurement systems. It is relatively easy to implement and provides fast intrinsic jitter measurements. Low frequency network analyzers are often employed to measure jitter transfer.

There are several limitations of the phase detector technique. This type of jitter measurement system usually consists of dedicated hardware, which only functions at specific transmission rates. Furthermore, a range of bandpass filters are needed for each hierarchical level. In addition, the accuracy of the jitter transfer measurement with a network analyzer may be insufficient to guarantee the specification is being met.* Finally, the technique requires an additional clock source as a reference for the phase detector.

Specific advantages of the 71501D jitter measurement technique

Sampler-based instruments offer a general purpose solution. These instruments typically operate by taking time samples of the data, then analyzing it using digital signal processing techniques. One such instrument is the 71501D jitter analyzer, which offers several distinct advantages. The analyzer provides automatic SONET/SDH jitter equipment measurement capability at 2488 Mb/s and 9953 Mb/s. The measurement technique employed is frequency agile, allowing the instrument to make jitter measurements from 50 Mb/s to greater than 12.5 Gb/s. A special version of the 71501D analyzer is available to perform jitter measurements for multiplexers and demultiplexers where the input rate and output rates are dissimilar. Furthermore, the 71501D analyzer also offers diagnostic measurements of the jittered clock waveform and spectrum, as well as the demodulated jitter waveform and spectrum.

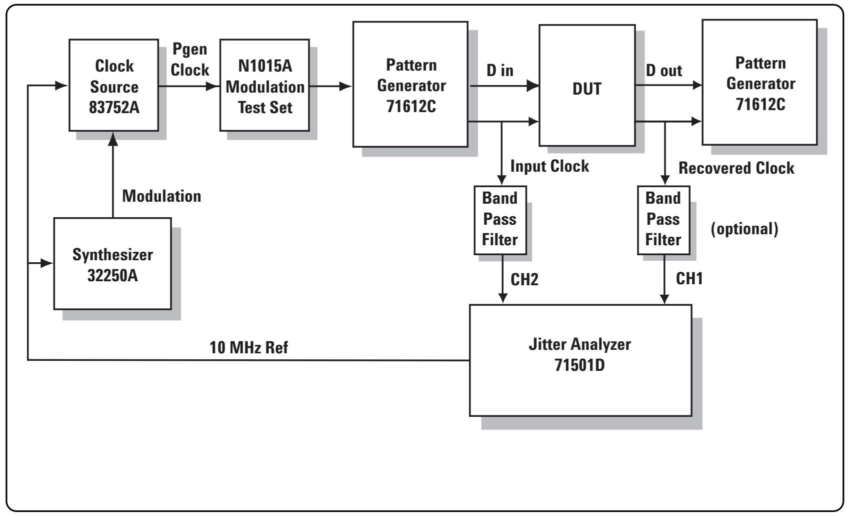


Figure 9. Configuration when using the 71501D analyzer

In addition, the 71501D analyzer performs eye diagram and extinction ratio measurements on digital waveforms.

The 71501D analyzer-based jitter measurement system is shown in Figure 9. The system configuration includes a 71612C 12 Gb/s pattern generator, error detector, 83752A clock source, and 32250A synthesizer which serves as the jitter modulation source. A jitter application program is downloaded into the instrument basic software of the 71501D analyzer. The program allows the 71501D analyzer to take control of all the other instruments in the jitter measurement system and to coordinate the measurements.

A jitter application specific menu (Figure 10) is provided with soft-

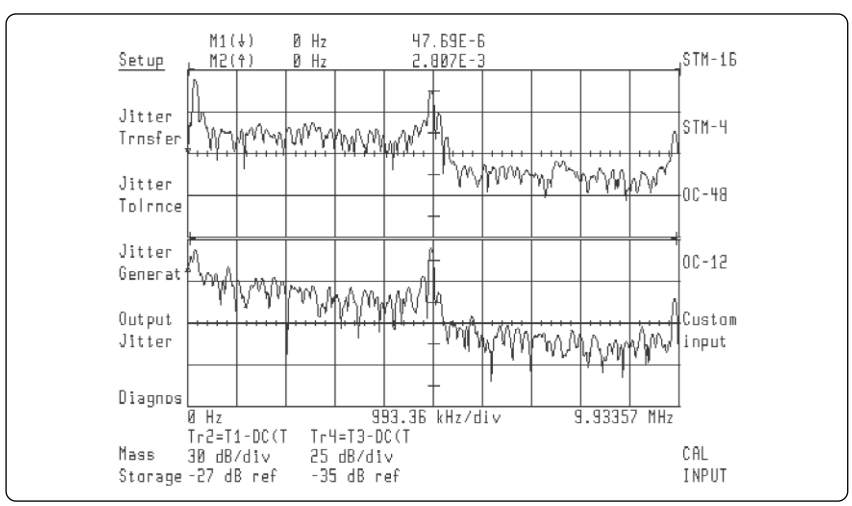


Figure 10. Jitter application menu

* The Agilent JS-1000, like the 71501D, is a frequency agile architecture, however it's accuracy is among the best.

keys to lead the user through the measurement procedure. First, the transmission rate and accompanying input jitter (tolerance) template is selected. SONET, SDH, or custom templates may be selected. Custom templates can be created, edited, and stored on a RAM card. A calibration routine is required to establish the recommended jitter levels that conform to the template prior to a jitter transfer or jitter tolerance measurement.

Figure 11 shows the capability of the jitter measurement system at 2.48832 Gb/s compared to the jitter tolerance masks for OC-48 and STM-16. The measurement range of the 71501D analyzer is shown, as well as the jitter modulation capability of the 83752A clock source. Both the jitter modulation and measurement capability exceed that required by the standards.

Similarly, Figure 12 shows the jitter modulation and measurement capability of the measurement system relative to the jitter tolerance templates for OC-12 and STM-4. Once again, this capability is sufficient to meet the requirements of the standard.

Jitter measurement range, in terms of the data rates, jitter rates and jitter magnitudes, is essentially dependent upon the clock source used. The standard clock source for the analyzer-based system is the 83752A, which is typically used for 9533 Mb/s and 2488 Mb/s compliance testing.

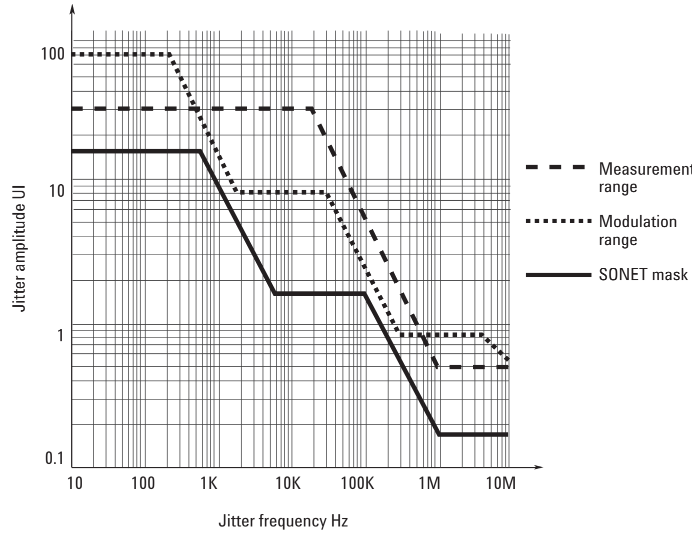


Figure 11. Jitter measurement characteristics (rate: 2.48832 Gb/s)

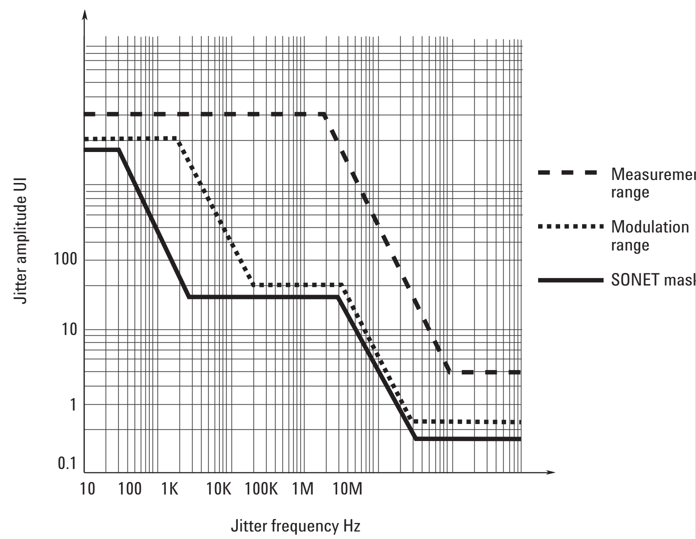


Figure 12. Jitter measurement characteristics (rate: 622.08 Mb/s)

Jitter tolerance measurement setup

The jitter tolerance measurement determines whether a test device or subsystem can transmit error-free data in the presence of jitter. The 71612C error detector monitors the recovered clock and regenerated data. Typically, an attenuator is placed in the input data path to reduce the signal power until the threshold of error generation is achieved. The attenuation is then reduced by 1 dB.

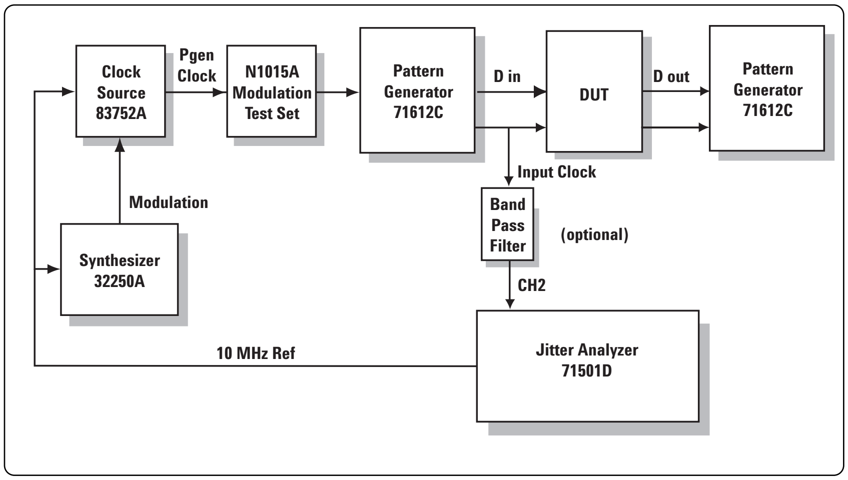


Figure 13. Setup for jitter tolerance measurement

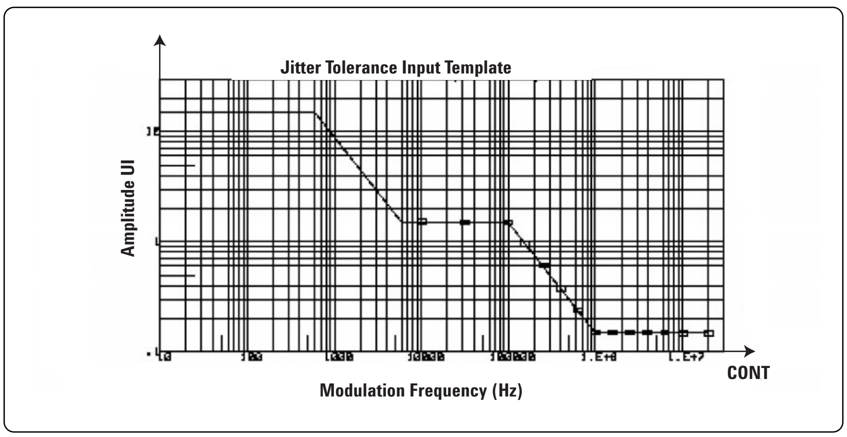


Figure 14. Results of a jitter tolerance test

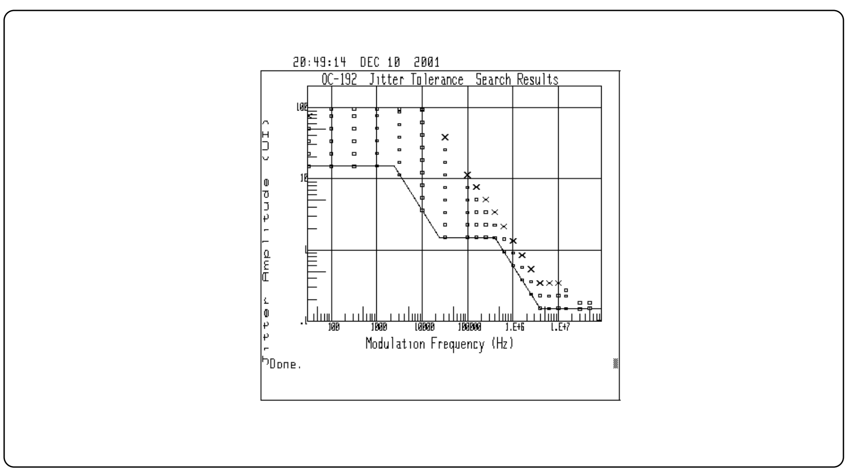


Figure 15. Jitter tolerance search results

Then, at a number of modulation frequencies, the amount of sinusoidal jitter corresponding to the input tolerance template is applied, while the error status is monitored. (Figure 13)

The plot in Figure 14 shows the jitter levels at each jitter measurement frequency, and whether or not errors were generated. The jitter frequencies and amplitude levels, along with pass/fail status can also be displayed in table format.

In addition to the jitter compliance test, it is often useful to determine by what margin a system or device exceeds the jitter tolerance template. The 71501D analyzer can automatically search for the jitter level at which tolerance failure threshold is reached. The search step size is user defined. The system will either increase jitter until the failure criteria is met, or until the maximum jitter generation capability of the system is reached. Failures, and thus the jitter tolerance margin level are indicated by an 'X'. (Figure 15)

Jitter transfer measurement setup

The jitter transfer measurement setup (Figure 16) is similar to the jitter tolerance measurement setup. The main difference is that the error detector is not required as we are now measuring the ratio of applied jitter to output jitter. The recovered clock signal from the device under test is routed to channel 1 of the analyzer while the applied jitter on the input clock signal is monitored on channel 2. This measurement technique works well for several reasons. First, jitter applied to the clock input of the 71612C pattern generator appears equally at its data and clock outputs, therefore any data test pattern can be used. In addition, the 71501D analyzer has two input channels that are sampled synchronously, allowing accurate phase measurements between the two channels.

Figure 17 shows an example of a jitter transfer measurement at a single jitter modulation frequency, 1.57 MHz. The data rate is 2488 Mb/s. The upper trace is the demodulated jitter spectrum of the input clock signal on Channel 2. The lower trace is the demodulated jitter spectrum of the recovered clock signal from the DUT measured at Channel 1. The ratio of the signal amplitudes at the jitter modulation frequency is the jitter transfer of the DUT at that frequency. The 71501D analyzer can make this measurement accurately because it simultaneously measures both the input and output jitter. (Figure 18)

After the jitter transfer is plotted, the specified transfer function for the selected standard transmission rate is over-laid. Any failures

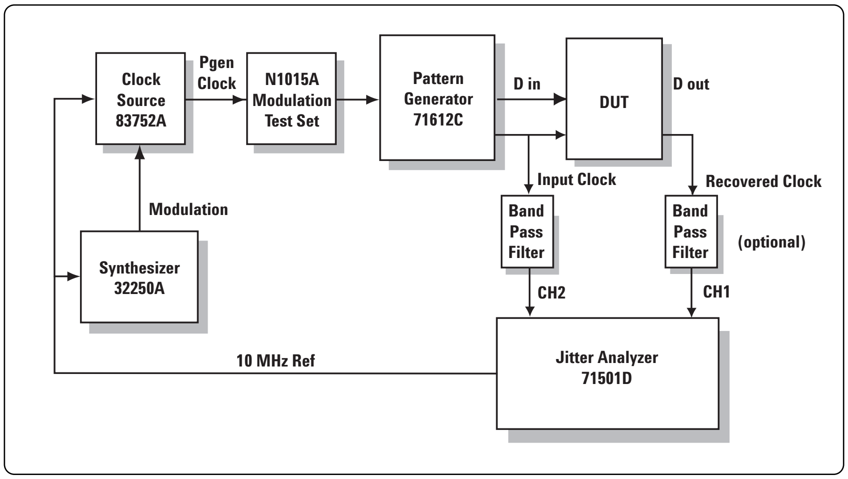


Figure 16. Setup for jitter transfer measurement

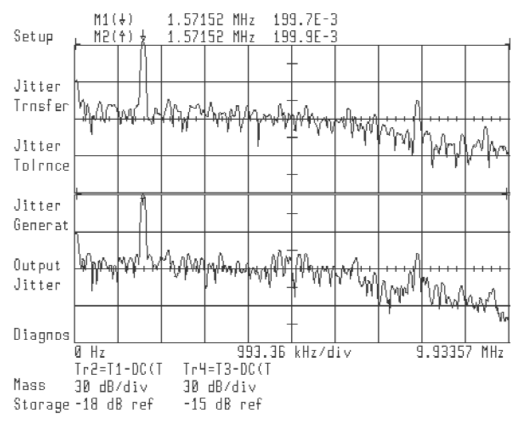


Figure 17. Example jitter transfer measurement

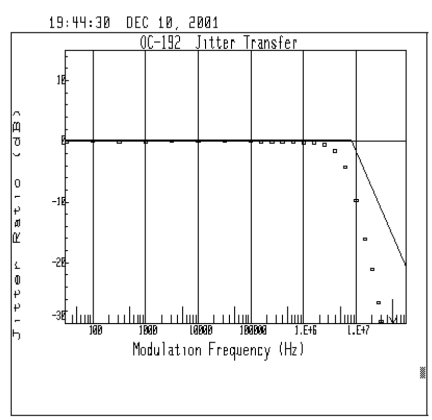


Figure 18. Plot of jitter transfer function

are noted. Here is a plot of jitter transfer of clock recovery circuit operating at 9533 Mb/s. The difference between the measured jitter transfer data and the specified transfer function can also be plotted, or a table can be displayed which lists all of the data.

The jitter test plate can be customized by raising or lowering the transfer function level (typically 0.1 dB). The frequency of the transfer template roll-off can also be user defined.

Jitter transfer for multiplexer and demultiplexer devices is a complex measurement. The input rates and output rates are dissimilar. However, the task is easily performed with the 71501D analyzer-based system. In Figure 19, testing a 1:32 mux, channel 2 of the 71501D analyzer (the reference channel) is set to receive a 155 Mb/s clock signal; whereas channel 1 receives the 4.98 Gbit output clock. This measurement is achieved because of the frequency agility of the analyzer-based system.

Intrinsic jitter measurement

The intrinsic jitter measurement setup (Figure 20) is similar to the jitter transfer setup, except there is no jittered input signal to the DUT. The intrinsic jitter on the recovered clock output of the DUT is monitored on Channel 1 of the 71501D analyzer. It should be noted that intrinsic jitter is essentially a noise measurement. A bandpass filter at the appropriate clock frequency is used to set the upper limit of the noise measurement bandwidth.

As previously stated, jitter generation is an intrinsic jitter measurement on a piece of network equipment, such as a regenerator, or a component. The standards specify the jitter spectrum be measured with a 12 kHz highpass filter. The 71501D analyzer implements this 12 kHz highpass characteristic in software with the corner frequency for the filter being adjustable. The bandlimited noise spectrum is then transformed to the time domain and displayed as shown here. Transformation to the time domain makes it possible to determine the peak-to-peak as well as RMS jitter values. (Figure 21)

The output jitter measurement technique is similar to the jitter generation measurement. However, in the case of output jitter, the measurement is intended to be performed at network interfaces. The output jitter specifications apply to line systems which may contain terminals, add-drop multiplexers and regenerators. Two measurement bandwidths with different low cut-off frequencies are required by the standards. The upper measurement frequency limit is set by the hardware filter.

The software filters set the lower measurement frequency limit. OC-192 recommends two

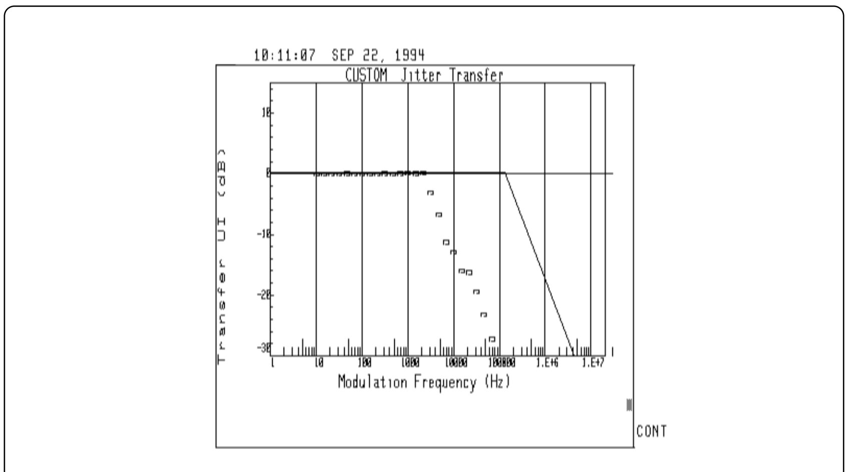


Figure 19. Results for custom jitter transfer measurement

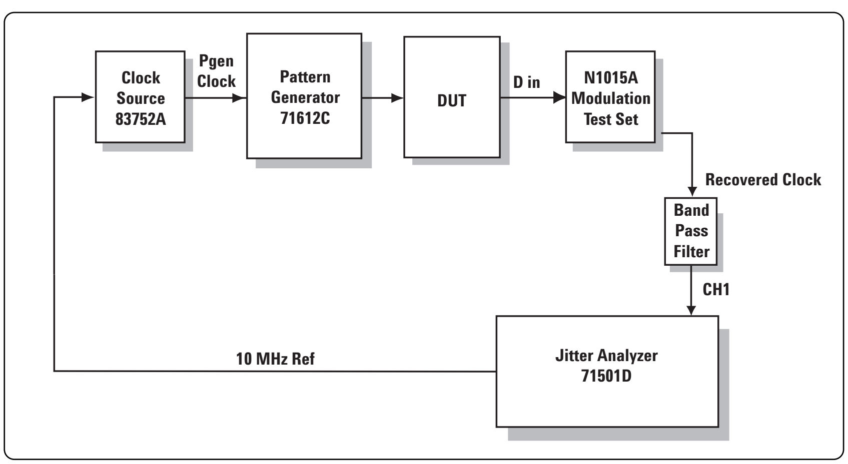


Figure 20. Setup for intrinsic jitter measurement

measurement bandwidths of 20 KHz to 80 MHz and 4 MHz to 80 MHz (see Figure 6). To fulfill the latter requirement, the 71501D is set to use a low cut-off frequency of 1 MHz. Measurements made in this fashion will guarantee network interface jitter compliance with only a slightly more stringent setting.

Shown in Figure 22 is the measurement performed on a clock recovery unit at 2488 Mb/s. Both bandwidths are measured automatically, and the results displayed in both peak-to-peak UI and rms UI. Note that to make this measurement at the interface of a line system, some form of broadband clock recovery unit is required to measure the jitter. The bandwidth of the broadband clock recovery unit should be significantly larger than the equipment in the network, to allow the jitter in the network to be measured.

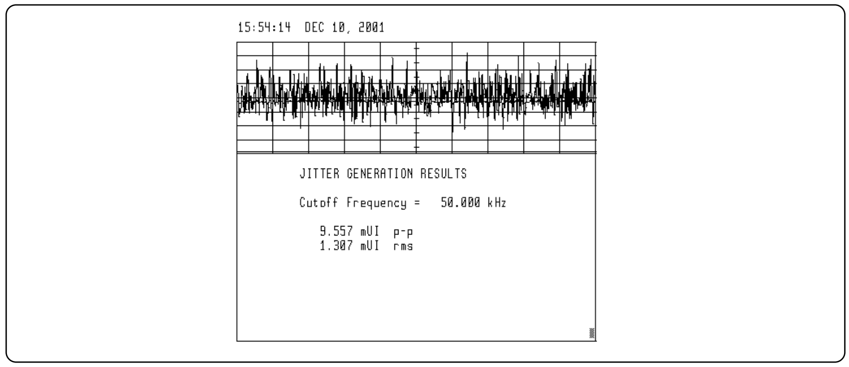


Figure 21. Example results for jitter generation measurement

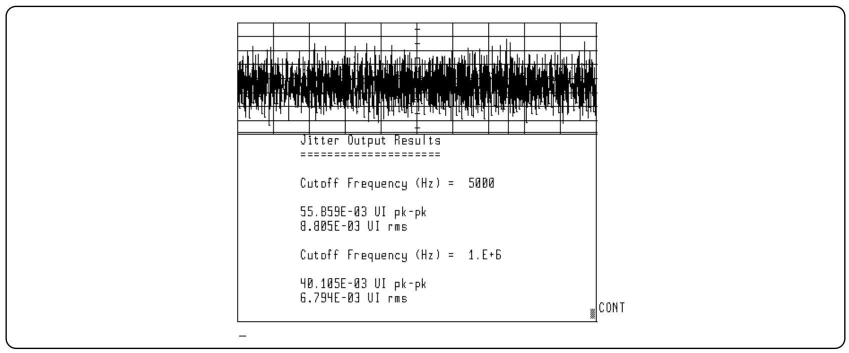


Figure 22. Example of jitter output results

71501D jitter analyzer

The unique architecture of the 71501D analyzer allows it to have the attributes of a digital sampling oscilloscope, an RF spectrum analyzer, and a modulation analyzer. This makes it very useful for a number of diagnostic measurements. In addition, it is a two channel instrument which is appropriate for this application. As shown in Figure 23, microwave samplers are used to down convert the input signal to a DC to 10 MHz intermediate frequency (IF), where the signal is digitized and appropriate digital signal processing (DSP) can be applied. The sample rate is nominally close to 20 MHz, but adjusts itself based on the incoming signal frequency, to optimally down convert the signal to the IF section. The internal DSP is used to perform fast fourier transforms (FFT's), inverse fast fourier transforms (IFFT's), and demodulation on the input signal.

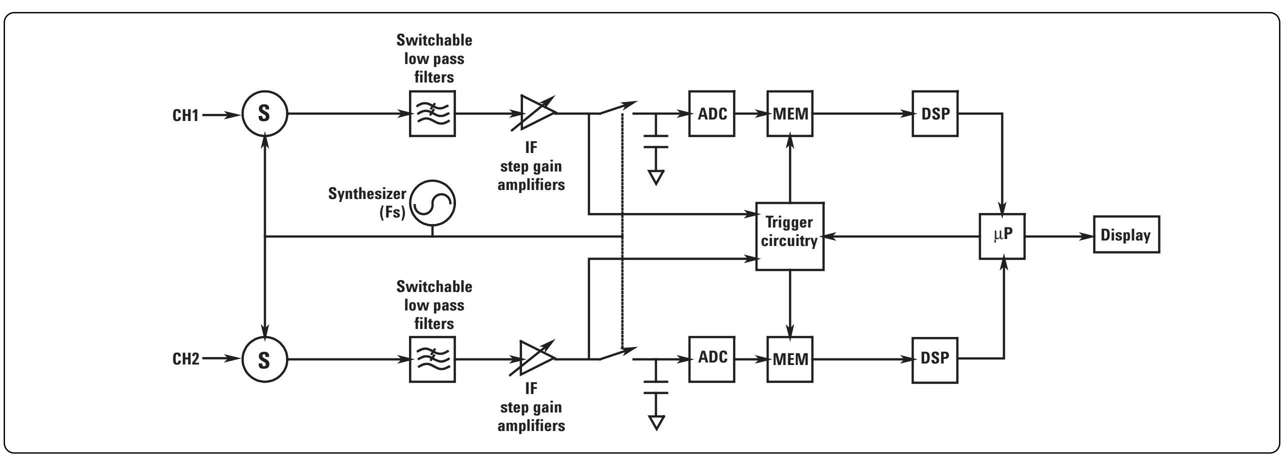


Figure 23. Block diagram of 71501D analyzer

Diagnostic capabilities of the 71501D jitter analyzer

- View demodulated jitter waveform and spectrum
- View clock waveform and spectrum
- Generate custom input tolerance templates
- Analyze intrinsic jitter with variable highpass filter

The 71501D analyzer may be unique in its ability to display the data, clock, and demodulated jitter waveforms and spectra. A mode is available to assist in the diagnosis of equipment failures, or with the development of the new components or systems, as each jitter modulation frequency or jitter amplitude can be examined.

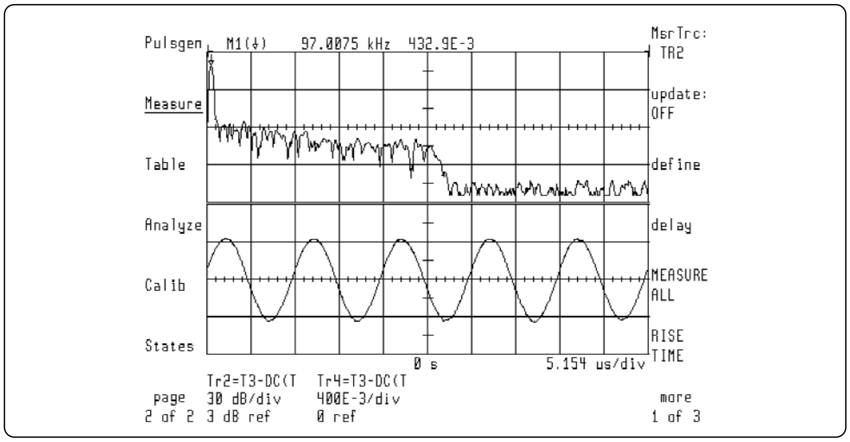


Figure 24. Display of the demodulated jitter spectrum and waveform

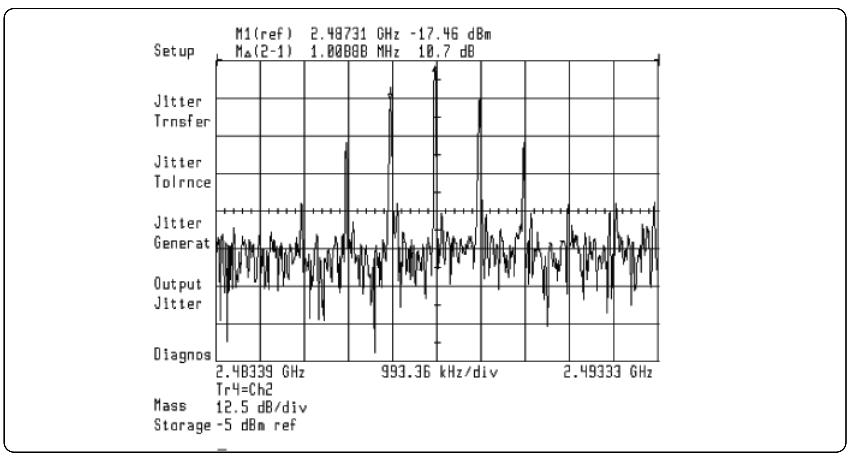


Figure 25. Display of sinusoidal jitter modulation present on the clock

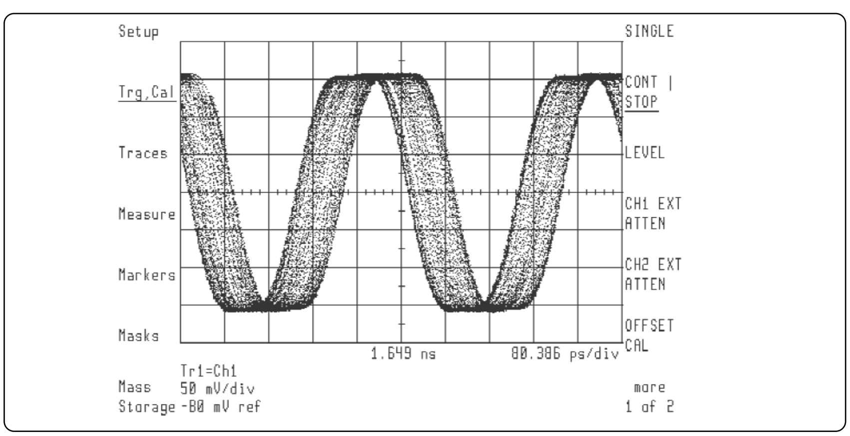


Figure 26. Display of clock waveforms with jitter

In Figure 24, the demodulated jitter spectrum and waveform of a sinusoidally modulated clock signal are displayed. The modulating frequency was approximately 97 kHz and the clock rate was 2488 Mb/s.

This capability may be useful in determining the relative contributions of random and systematic jitter. As was previously mentioned, custom tolerance templates can be constructed to analyze error performance. In addition, adjustable software highpass filter aid intrinsic noise analysis.

The sinusoidal jitter modulation present on the clock can be displayed in the frequency domain similar to the display of an RF spectrum analyzer. The trace in Figure 25 shows the spectrum of the clock at 2.48832 GHz being sinusoidally modulated at a 1 MHz rate. The sidebands, as expected, have the appropriate Bessel amplitudes corresponding to FM modulation.

The clock and data waveforms can also be displayed similar to a digital sampling oscilloscope. A full set of histogram functions are available to measure timing jitter. In addition, eye diagram mask and extinction ratio measurement can be performed. The trace in Figure 26 shows a display of a jittered clock waveform. The transmission rate was 2488 Mb/s and the jitter frequency and amplitude were 10 kHz and .2 UI respectfully.

Summary

Jitter is an important parameter that must be controlled in transmission system to minimize bit errors. Equipment level standard specifications, such as ITU-T G.958 have been developed to insure that network equipment will operate within the appropriate jitter budget. The 71501D jitter analyzer can aid equipment manufacturers by performing industry standard jitter measurements such as jitter tolerance, jitter transfer, jitter generation, and output jitter at 9533 Mb/s and 2488 Mb/s. Its measurement capability is frequency-agile from less than 50 Mb/s to greater than 12.5 Gb/s. Custom input tolerance templates can be constructed, and variable bandwidth noise measurements can be performed. To aid equipment designers, the 71501D analyzer has significant diagnostic capability that allows the demodulated jitter spectrum and waveform to be observed. In addition, it can perform extensive eye diagram and extinction ratio measurements.

Configuration information

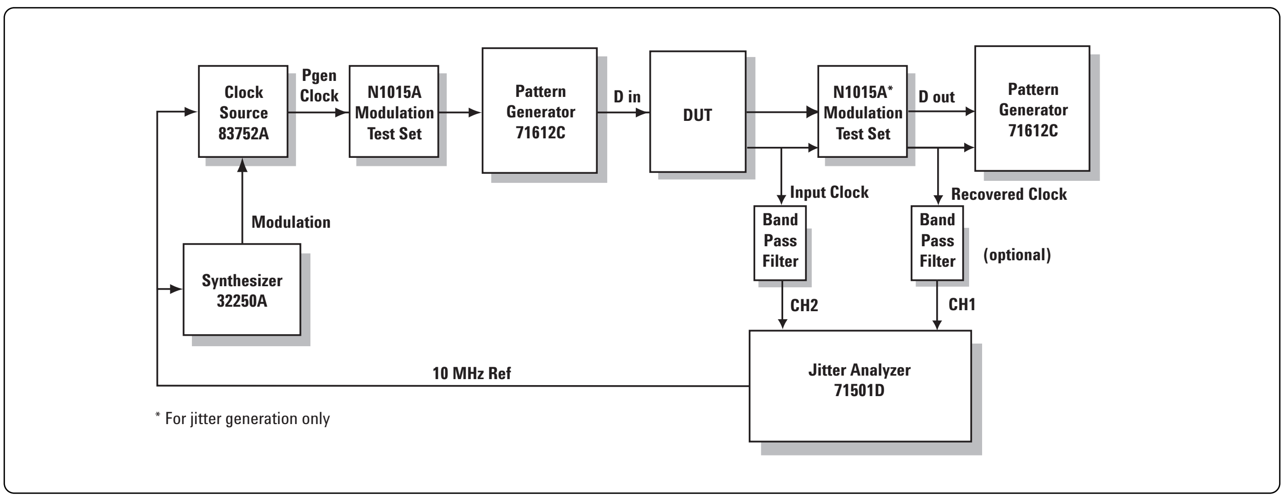


Figure 27. System configuration for the 50Mb/s to 12.5 Gb/s

71501D analyzer-based system configuration

The standard configuration of the 71501D analyzer-based jitter analysis system is capable of operating from 50 Mb/s to 12.5 Gb/s. It is capable of SDH/SONET compliance measurements at 9533 Mb/s and 2488 Mb/s and must include the following equipment:

- 71501D jitter analyzer includes:
  70004A display mainframe.
  70820A microwave transition analyzer with expanded memory.
  Standard jitter measurement software.
  Bandpass filter for 9533 Mb/s and 2488 Mb/s testing.
  Cables and accessories for system phase-locking.
- 33250A synthesized function generator (jitter source).
- 83752A clock source.

83752A clock source

The 83752A synthesized sweep generator is a general purpose signal generator that operates from 10 MHz to 20 GHz. Jitter is independent of data rate, thus this clock source can be used over the full range of the 71501D analyzer-based system (50 Mb/s to beyond 12.5 Gb/s). It also has a jitter bandwidth approaching 10 MHz, approximately double that of the 70340A clock source. Maximum level of jitter that can be generated with the 83752A generator is approximately 16 UI.

86130A BitAlyzer®

This error performance analyzer is supported by the 71501D jitter analyzer system.

70340A clock source

The 70340A is the standard clock source used with the 71612C error performance analyzer. It operates from 1 to 12.5 Gb/s. Jitter generation capability is constant with data rate. It can achieve over 30 UI of jitter over the frequency range of 70 Hz to 60 KHz. However, the jitter modulation range is approximately 5 MHz. It is useful for general jitter measurements, but is not capable of operating to the full 20 MHz required for compliance testing at 2.488 Gb/s.

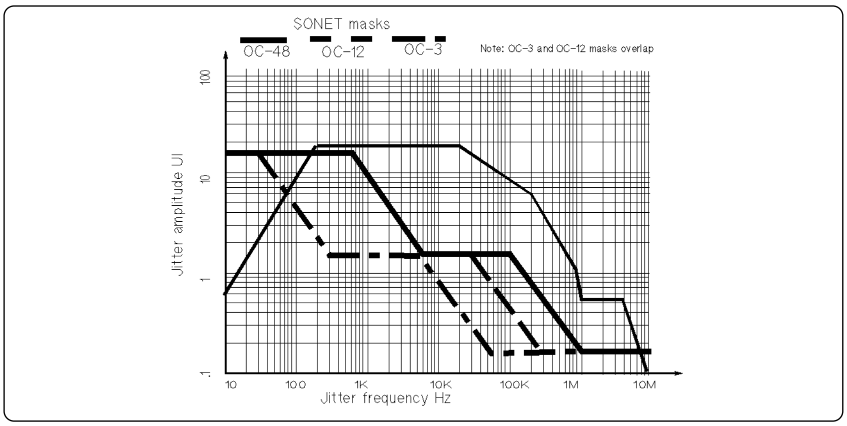


Figure 30. 83752A clock source modulation capability

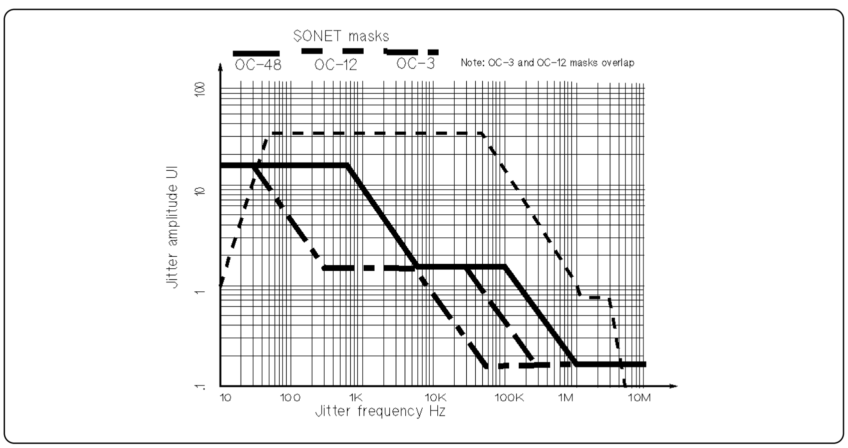


Figure 31. 70340A clock source modulation capability

References

ITU-T recommendation G.958, "Digital line systems based on the synchronous digital hierarchy for use on optical fibre cables."

ITU-T recommendation G.825, "The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy."

ANSI T1X1.3/93-006R2, "Synchronous Optical Network (SONET): Jitter at network interfaces."

Bellcore TA-NWT-00253, "Synchronous Optical Network (SONET) transport systems: Common generic criteria."

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Printed in USA March 22, 2002
5988-5610EN

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